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| 09/788,105      | 02/16/2001  | Jay E. Uglow         | LAM1P106D           | 2844             |

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EXAMINER

PHAM, THANHHA S

| ART UNIT | PAPER NUMBER |
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2813

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/788,105

Applicant(s)

UGLOW ET AL.

Examiner

Thanhha Pham

Art Unit

2813

MLW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 21-24 and 26-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 41 is/are allowed.
- 6) ☒ Claim(s) 21-24 and 26-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

This Office Action responses to Applicant's Amendment in Paper No. 16 dated 9/29/03.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**1. Claims 21 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh [US 6,225,207] in view of Yu et al [US 6,187,663].**

➤ With respect to claim 21, Parikh (fig 7F and col 1-19) discloses a multi-layer dielectric layer over a substrate for use in dual-damascene applications comprising:

a barrier layer (712: layer 712 of fig 7F defines conductive path, signal line 752, to the substrate 710; layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being contact with the conductive path 752) disposed over the substrate (710);

an inorganic dielectric layer (714, PECVD-SiO<sub>2</sub> or F-SiO<sub>2</sub>, col 13 lines 39-41) disposed over the barrier layer; and

a low dielectric constant layer (716, col 13 lines 42-57) disposed directly over and in direct contact with the inorganic dielectric layer (714);

wherein the low dielectric constant layer (716) is configured to receive metallization line trenches (736) to define metallization line layer (fig 7E-7F, col 13 lines 3-15: dual damascene 736/740 is filled by metal therefore the metallization line layer is defined in the metallization line trench 736) and the inorganic dielectric layer is configured to receive vias (740) during a dual damascene process.

Parikh et al is silent about the inorganic dielectric layer of PECVD-SiO<sub>2</sub> or F-SiO<sub>2</sub> having a dielectric constant of about 4. However, the claimed range of dielectric constant of about 4 is considered to involve routine optimize routine optimization while has been held to be within the level of ordinary skill in the art. The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Moreover, Yu et al (fig 6, col 3 lines 35-39) teaches the inorganic dielectric layer (4) of fluorine doped silicon dioxide (FSG) having the dielectric constant of about 4 (3.5-3.7). Therefore, it would have been obvious for those skilled in the art to use the inorganic dielectric layer having the dielectric constant of about 4 as being claimed, per

taught by Yu et al, to define the via in the dual damascene application of Parikh.

Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.).

➤ With respect to claim 36, Parikh (fig 7F and col 1-19) discloses a dielectric structure for dual-damascene applications comprising:

a barrier layer (712: layer 712 of fig 7F defines conductive path, signal line 752, to the substrate 710; layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being contact with the conductive path 752) disposed over as a base (710);

an inorganic dielectric layer of a fluorine doped oxide (714, F-SiO<sub>2</sub>, col 13 lines 39-41) disposed over the barrier layer;

a low dielectric constant layer of a carbon-doped oxide (716, DVS-BCB, col 13 lines 42-57) disposed directly over and in direct contact with the inorganic dielectric layer (714);

wherein the low dielectric constant layer (716) is configured to receive metallization line trenches (736) to define metallization line layer (fig 7E-7F, col 13 lines 3-15: dual damascene 736/740 is filled by metal therefore the metallization line layer is defined in the metallization line trench 736) and the inorganic dielectric layer is configured to receive vias (740) during a dual damascene process.

Parikh does not expressly teach the barrier layer being disposed over a base dielectric. Instead, Parikh teaches the barrier layer (712) is generally disposed on a base (710) of a semiconductor substrate including IC elements and interconnects.

However, Yu et al discloses a dielectric structure for dual damascene application comprising the barrier (3, fig 6) disposed over the dielectric base (1) for forming interconnection between metallization line in dual damascene structure to an interconnect (2) in the dielectric base (1).

Therefore, it would have been obvious for those skilled in the art to modify the dielectric structure for dual damascene application of Parikh by using the dielectric base on which the barrier is disposed over as being claimed, per taught by Yu et al, to provide interconnection between metallization line in dual damascene structure to the interconnect in the dielectric base as a design of a semiconductor being needed.

➤ With respect to claims 37-40, the claimed ranged thickness of the inorganic dielectric layer and the low dielectric layer are considered to involve routine experimentation while has been held to be within the level of ordinary skill in the art. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1998) (discovery of optimum value of result effective

variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

**2. Claims 21 and 31-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh [US 6,225, 207] in view of Applicant's Admitted Prior Art (APA).**

➤ With respect to claim 21, Parikh (fig 7F and col 1-19) discloses a multi-layer dielectric layer over a substrate for use in dual-damascene applications comprising:

a barrier layer (712: layer 712 of fig 7F defines conductive path, signal line 752, to the substrate 710; layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being contact with the conductive path 752) disposed over the substrate (710);

an inorganic dielectric layer (714, PECVD-SiO<sub>2</sub>, col 13 lines 39-41) disposed over the barrier layer; and

a low dielectric constant layer (716, col 13 lines 42-57) disposed directly over and in direct contact with the inorganic dielectric layer (714);

wherein the low dielectric constant layer (716) is configured to receive metallization line trenches (736) to define metallization line layer (fig 7E-7F, col 13 lines 3-15: dual damascene 736/740 is filled by metal therefore the metallization line layer is defined in the metallization line trench 736) and the inorganic dielectric layer is configured to receive vias (740) during a dual damascene process.

Parikh et al is silent about the inorganic dielectric layer of PECVD-SiO<sub>2</sub> having a dielectric constant of about 4. However, the claimed range of dielectric constant of about 4 is considered to involve routine optimize routine optimization while has been held to be within the level of ordinary skill in the art. The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Moreover, APA ( fig 1 and specification page 2) teaches using the inorganic dielectric layer (18a, undoped TEOS oxide) having the dielectric constant of about 4 (4.1) configured to receive vias during a dual damascene process. Therefore, it would have been obvious for those skilled in the art to modify the multi-layer dielectric layer of Parikh by using the inorganic dielectric layer having the dielectric constant of about 4 as being claimed, per taught by APA, to define the via in the dual damascene application in a semiconductor device. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list



and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.).

➤ With respect to claim 31, Parikh (fig 7F and col 1-19) discloses a multi-layer inter-metal dielectric semiconductor structure comprising:

a barrier layer (712: layer 712 of fig 7F defines conductive path, signal line 752, to the substrate 710; layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being contact with the conductive path 752) disposed over as a base (710);

an inorganic dielectric layer (714, PECVD-SiO<sub>2</sub>, col 13 lines 39-41) disposed over the barrier layer;

a low dielectric constant layer of a carbon-doped oxide (716, DVS-BCB, col 13 lines 42-57) disposed directly over and in direct contact with the inorganic dielectric layer (714);

wherein the low dielectric constant layer (716) is configured to receive metallization line trenches (736) to define metallization line layer (fig 7E-7F, col 13 lines 3-15: dual damascene 736/740 is filled by metal therefore the metallization line layer is defined in the metallization line trench 736) and the inorganic dielectric layer is configured to receive vias (740) during a dual damascene process.

Parikh does not expressly teach:

- a) the barrier layer (712) being disposed over a base dielectric.

Instead, Parikh teaches the barrier layer (712) is generally disposed on a base (710) of a semiconductor substrate including IC elements and interconnects; and

- b) the inorganic dielectric layer (714) being of an undoped TEOS oxide.

Regarding to a), APA (fig 1, specification pages 2-3) discloses a multi-layer inter-metal dielectric semiconductor structure using barrier (16a) disposed over the dielectric base (10) for forming interconnection between metallization line in dual damascene structure to an interconnect (12/14) in the dielectric base (10). Therefore, it would have been obvious for those skilled in the art to modify the dielectric structure for dual damascene application of Parikh by using the dielectric base on which the barrier is disposed over as being claimed, per taught by APA, to provide interconnection between metallization line in dual damascene structure to the interconnect in the dielectric base as a design of a semiconductor being needed.

Regarding to b), undoped TEOS oxide is a known inorganic material in a multi-layer inter-metal dielectric semiconductor structure that is used to configure to receive vias during a dual damascene process. See APA as an evidence that shows using the inorganic dielectric layer of the undoped TEOS oxide (18a, fig 1) to define vias in dual damascene application. Therefore, it would have been obvious for those skilled in the art to modify the multi-layer inter-metal dielectric semiconductor structure of Parikh by using the undoped TEOS oxide as the known material, per taught by APA, for the inorganic dielectric layer to receive vias in dual damascene application. Selection of a

known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.).

➤ With respect to claim 36, Parikh (fig 7F and col 1-19) discloses a dielectric structure for dual-damascene applications comprising:

a barrier layer (712: layer 712 of fig 7F defines conductive path, signal line 752, to the substrate 710; layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being contact with the conductive path 752) disposed over as a base (710);

an inorganic dielectric layer of a fluorine doped oxide (714, F-SiO<sub>2</sub>, col 13 lines 39-41) disposed over the barrier layer;

a low dielectric constant layer of a carbon-doped oxide (716, DVS-BCB, col 13 lines 42-57) disposed directly over and in direct contact with the inorganic dielectric layer (714);

wherein the low dielectric constant layer (716) is configured to receive metallization line trenches (736) to define metallization line layer (fig 7E-7F, col 13 lines 3-15: dual damascene 736/740 is filled by metal therefore the metallization line layer is defined in the metallization line trench 736) and the inorganic dielectric layer is configured to receive vias (740) during a dual damascene process.

Parikh does not expressly teach the barrier layer being disposed over a base dielectric. Instead, Parikh teaches the barrier layer (712) is generally disposed on a base (710) of a semiconductor substrate including IC elements and interconnects.

However, APA (fig 1, specification pages 2-3) discloses a dielectric structure for dual damascene applications using barrier (16a) disposed over the dielectric base (10) for forming interconnection between metallization line in dual damascene structure to an interconnect (12/14) in the dielectric base (10). Therefore, it would have been obvious for those skilled in the art to modify the dielectric structure for dual damascene application of Parikh by using the dielectric base on which the barrier is disposed over as being claimed, per taught by APA, to provide interconnection between metallization line in dual damascene structure to the interconnect in the dielectric base as a design of a semiconductor being needed.

➤ With respect to claims 32-35 and 37-40, the claimed ranged thickness of the inorganic dielectric layer and the low dielectric layer are considered to involve routine experimentation while has been held to be within the level of ordinary skill in the art. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1998) (discovery of optimum value of result effective

variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

**3. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being being unpatentable over Wang et al [US 6,255,735] in view of Applicant's Admitted Prior Art (APA).**

➤ With respect to claim 21, Wang et al , fig 11 and cols 1-8, discloses a multi-layer dielectric layer/structure over a substrate for dual damascene applications comprising:

a barrier layer (12, col 5 lines 28-31) disposed over the substrate (10);

an inorganic dielectric layer (14, col 5 lines 40-41) disposed over the barrier layer; and

a low dielectric constant layer (18, col 5 lines 51-67 and col 6 lines 1-11) disposed directly over and in directly contact with the inorganic dielectric layer (14);

wherein the low dielectric constant layer(18) is configured to receive metallization line trenches to define a metallization line layer and the inorganic dielectric layer is configured to receive vias during a dual damascene process.

Wang et al is silent about the inorganic dielectric layer having a dielectric constant of about 4. However, the claimed range of dielectric constant of about 4 is considered to involve routine optimize routine optimization while has been held to be within the level of ordinary skill in the art. The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang,

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40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Moreover, APA ( fig 1 and specification page 2) teaches using the inorganic dielectric layer (18a, undoped TEOS oxide) having the dielectric constant of about 4 (4.1) configured to receive vias during a dual damascene process. Therefore, it would have been obvious for those skilled in the art to modify the multi-layer dielectric layer of Parikh by using the inorganic dielectric layer having the dielectric constant of about 4 as being claimed, per taught by APA, to define the via in the dual damascene application in a semiconductor device. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.).

➤ With respect to claim 22, Wang et al (col 5 lines 26-31) discloses the barrier layer (12, silicon nitride) is one of a silicon nitride layer and a silicon carbide layer.

➤ With respect to claim 23, Wang et al (col 5 lines 40-41) discloses the inorganic dielectric layer (14, SiOF) is one of an undoped TEOS layer and fluorine doped oxide.

**4. Claims 24 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al [US 6,255,735] in view of APA as applied to claim 23 above, and further in view of Usami [US 6,077,574].**

➤ With respect to claim 24, Wang et al in view of APA substantially discloses the claimed multi-layer dielectric layer over a substrate for use in dual-damascene

application except teaching the low dielectric constant layer being of a carbon doped oxide.

However, Usami teaches using the carbon-doped oxide layer would provide a better low constant dielectric layer with good resistance to moisture and heat.

Therefore, it would have been obvious for those skilled in the art to modify the multi-layer dielectric layer of Wang et al in view of APA by using the low constant dielectric layer of carbon doped oxide, as taught by Usami, to form the multi-layer dielectric layer with a good characteristics of low RC, good resistance to moisture and resistance to heat.

- With respect to claim 26, Wang et al (col 5 lines 51-67) discloses the inorganic dielectric layer (14) has different material properties than the low dielectric constant layer (18).
- With respect to claim 27-30, the claimed ranged thickness of the inorganic dielectric layer and the low dielectric layer are considered to involve routine experimentation while has been held to be within the level of ordinary skill in the art. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective



variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

**5. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al [US 6,255,735] in view of APA and Usami [US 6,077,574].**

➤ With respect to claim 31, Wang et al , fig 11 and cols 1-8, discloses a multi-layer inter-metal dielectric semiconductor structure comprising:

a barrier layer (12, col 5 lines 28-31) disposed over a metal interconnection region (10);

an inorganic dielectric layer (14, SiOF, col 5 lines 40-41) disposed over the barrier layer; and

a low dielectric constant layer (18, col 5 lines 51-67 and col 6 lines 1-11) disposed directly over and in directly contact with the inorganic dielectric layer (14);

wherein the low dielectric constant layer(18) is configured to receive metallization line trenches to define a metallization line layer and the inorganic dielectric layer is configured to receive vias during a dual damascene process.

Wang et al does not expressly teach:

- a) the barrier layer being disposed over a based dielectric;
- b) the inorganic dielectric layer being formed of an undoped TEOS oxide; and
- c) the low dielectric constant layer being formed of a carbon doped oxide.

Regarding to a), APA (fig 1, specification pages 2-3) discloses a multi-layer inter-metal dielectric semiconductor structure using barrier (16a) disposed over the dielectric base (10) for forming interconnection between metallization line in dual damascene structure to an interconnect (12/14) in the dielectric base (10). Therefore, it would have been obvious for those skilled in the art to modify the dielectric structure for dual damascene application of Wang et al by using the dielectric base on which the barrier is disposed over as being claimed, per taught by APA, to provide interconnection between metallization line in dual damascene structure to the interconnect in the dielectric base as a design of a semiconductor being needed.

Regarding to b), undoped TEOS oxide is a known inorganic material in a multi-layer inter-metal dielectric semiconductor structure that is used to configure to receive vias during a dual damascene process. See APA as an evidence that shows using the inorganic dielectric layer of the undoped TEOS oxide (18a, fig 1) to define vias in dual damascene application. Therefore, it would have been obvious for those skilled in the art to modify the multi-layer inter-metal dielectric semiconductor structure of Wang et al by using the undoped TEOS oxide as the known material, per taught by APA, for the inorganic dielectric layer to receive vias in dual damascene application. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.).

Regarding to c), Usami teaches using the carbon-doped oxide layer would provide a better low constant dielectric layer with good resistance to moisture and heat. Therefore, it would have been obvious for those skilled in the art to modify the multi-layer inter-metal dielectric semiconductor structure of Wang et al in view of APA by using the low constant dielectric layer of carbon doped oxide, as taught by Usami, to form the multi-layer inter-metal dielectric semiconductor structure with a good characteristics of low RC, good resistance to moisture and resistance to heat.

➤ With respect to claim 36, Wang et al , fig 11 and cols 1-8, discloses a dielectric structure for dual damascene applications comprising:

a barrier layer (12, col 5 lines 28-31) disposed over a metal interconnection region (10);

an inorganic dielectric layer of a fluorine doped oxide (14, SiOF, col 5 lines 40-41) disposed over the barrier layer; and

a low dielectric constant layer (18, col 5 lines 51-67 and col 6 lines 1-11) disposed directly over and in directly contact with the inorganic dielectric layer (14);

wherein the low dielectric constant layer(18) is configured to receive metallization line trenches to define a metallization line layer and the inorganic dielectric layer is configured to receive vias during a dual damascene process.

Wang et al does not expressly teach:

- a) the barrier layer being disposed over a based dielectric; and
- b) the low dielectric constant layer being formed of a carbon doped oxide.

Regarding to a), APA (fig 1, specification pages 2-3) discloses a dielectric structure for dual damascene applications using barrier (16a) disposed over the dielectric base (10) for forming interconnection between metallization line in dual damascene structure to an interconnect (12/14) in the dielectric base (10). Therefore, it would have been obvious for those skilled in the art to modify the dielectric structure for dual damascene application of Wang et al by using the dielectric base on which the barrier is disposed over as being claimed, per taught by APA, to provide interconnection between metallization line in dual damascene structure to the interconnect in the dielectric base as a design of a semiconductor being needed.

Regarding to b), Usami teaches using the carbon-doped oxide layer would provide a better low constant dielectric layer with good resistance to moisture and heat. Therefore, it would have been obvious for those skilled in the art to modify the dielectric structure for dual damascene applications of Wang et al in view of APA by using the low constant dielectric layer of carbon doped oxide, as taught by Usami, to form the dielectric structure with a good characteristics of low RC, good resistance to moisture and resistance to heat in a semiconductor device.

➤ With respect to claims 32-35 and 37-40, the claimed ranged thickness of the inorganic dielectric layer and the low dielectric layer are considered to involve routine experimentation while has been held to be within the level of ordinary skill in the art. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

***Allowable Subject Matter***

6. Claim 41 is allowed.
7. The following is a statement of reasons for the indication of allowable subject matter: Recorded Prior Art fails to teach a multi-layer dielectric layer over a substrate for use in dual-damascene applications comprising: an inorganic dielectric layer of a fluorine doped oxid) disposed over the barrier layer, the inorganic dielectric layer having a first thickness; and a low dielectric constant layer of a carbon doped oxide disposed directly over and in direct contact with the inorganic dielectric layer, the low dielectric constant layer having a second thickness and defining metallization line layer; wherein metallization lines are formed in a first portion of the second thickness of the low dielectric constant layer, and a via path is configured to be defined in an entire portion of the first thickness of the inorganic dielectric layer and in at least a portion of the second thickness of the low dielectric constant layer as characteristics in claim 41.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172 (before 02/05/04) or (571) 272-1696 (after 02/05/04) The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached on (703) 308-4940 (before 02/05/04) or

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(571) 272-1702 (after 02/05/04). The fax phone number for the organization where this application or proceeding is assigned is (703) 308-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A handwritten signature in black ink, appearing to read 'Jack Chen', with a long horizontal line extending to the right.

**JACK CHEN**  
**PRIMARY EXAMINER**

Thanhha Pham